Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	286	(@pd>"20000505" and ((((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) not ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503"))) or (@pd>"20000505" and (((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector))))) or (@pd>"20000505" and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) or (@pd>"20000505" and (((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))) and @ad<"19950503")) or (@pd>"20000505" and ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503")) or (@pd>"20000505" and (((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)))	US-PGPUB; USPAT	OR	OFF	2005/09/18 15:02
L2	2264027	@ad<"19950503" or @rlad<"19950503"	US-PGPUB; USPAT	OR	OFF	2005/09/18 15:03
L3	11	l2 and l1	US-PGPUB; USPAT	OR	OFF	2005/09/18 15:03
L4	6338	(programm$3 near2 (logic or array) or fpga or fga)and l2	USPAT	OR	ON	2005/09/18 15:04
L5	452	(sFg or cfgs or (storage$1 near2 element$1)) and l4	USPAT	OR	ON	2005/09/18 15:05

L6	152	(pair or double or two) near5 (block$1 or bank$1) and l5	USPAT	OR	ON	2005/09/18 15:05
L7	32	(programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503" and l6	USPAT	OR	OFF	2005/09/18 15:05
L8	14	(((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)) and l6	USPAT	OR	OFF	2005/09/18 15:06
L9	62	((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))) and @ad<"19950503"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	OFF	2005/09/18 15:07
S2	369	VECTOR SAME (RECONFIGUR$5 OR CONFIGUR$5) AND "712"/$. CCLS.	USPAT	OR	OFF	2005/09/18 15:01
S3	225	VECTOR WITH (RECONFIGUR$5 OR CONFIGUR$5) AND "712"/$. CCLS.	USPAT	OR	OFF	2002/01/25 11:06
S4	31	VECTOR WITH (RECONFIGUR$5 OR CONFIGUR$5) AND 712/10-14.CCLS.	USPAT	OR	OFF	2002/01/25 11:28
S5	100	HYPERCUBE WITH TORUS	USPAT	OR	OFF	2002/01/25 11:23
S6	26	HYPERCUBE WITH TORUS SAME DIMENSION	USPAT	OR	OFF	2002/01/25 11:27
S7	16	(FOLD$3 WITH ARRAY) AND 712/10-14.CCLS.	USPAT	OR	OFF	2002/01/25 11:30
S8	2	(FOLD$3 WITH ARRAY) AND 712/10-14.CCLS. AND TORUS SAME HYPERCUBE	USPAT	OR	OFF	2002/01/25 12:19
S9	4	tanaka.in. and tasks.ti.	EPO; DERWENT	OR	OFF	2005/09/17 17:17
S10	90	btr.as.	USPAT	OR	OFF	2002/01/27 10:11
S11	0	btr.as. and ting.as.	USPAT	OR	OFF	2005/09/17 17:19
S12	8	btr.as. and ting.in.	USPAT	OR	OFF	2002/01/27 10:17
S13	1	"5894228".pn.	USPAT	OR	OFF	2002/01/27 10:18
S14	11012	programm$3 near2 (logic or array) or fpga or fga	USPAT	OR	ON	2005/09/18 15:04
S15	63851	(configur? near3 (function or generat$))".ab", ti, "clm."	USPAT	OR	ON	2002/01/27 10:59

S16	104056	(pair or double or two) near5 (block$1 or bank$1)	USPAT	OR	ON	2005/09/18 15:05
S17	17530	(sFg or cfgs or (storage$1 near2 element$1))	USPAT	OR	ON	2005/09/18 15:04
S18	6156	switch near3 matrix	USPAT	OR	ON	2002/01/27 11:02
S19	38006	(memory or passgate) near5 (array or vector)	USPAT	OR	ON	2002/01/27 11:03
S20	168	(programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))	USPAT	OR	ON	2002/01/27 11:03
S21	2142203	@ad<"19950503"	USPAT	OR	ON	2002/01/27 11:04
S22	64	((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))) and @ad<"19950503"	USPAT	OR	OFF	2005/09/18 15:07
S23	218	(programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503"	USPAT	OR	OFF	2005/09/18 15:05
S24	297	((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)	USPAT	OR	OFF	2002/01/27 11:11
S25	62	(((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector))	USPAT	OR	OFF	2005/09/18 15:05
S26	48	((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))	USPAT	OR	OFF	2002/01/27 11:13

S27	41	(((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) not ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503")	USPAT	OR	OFF	2005/09/18 15:06
S28	312576	@pd>"20000505"	USPAT	OR	OFF	2002/01/27 11:14
S29	2	@pd>"20000505" and ((((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) not ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503"))	USPAT	OR	OFF	2002/01/27 11:14
S30	2	@pd>"20000505" and (((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector))))	USPAT	OR	OFF	2002/01/27 11:14
S31	4	@pd>"20000505" and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))	USPAT	OR	OFF	2002/01/27 11:14
S32	0	@pd>"20000505" and (((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))) and @ad<"19950503")	USPAT	OR	OFF	2002/01/27 11:15
S33	3	@pd>"20000505" and ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503")	USPAT	OR	OFF	2002/01/27 11:15

S34	36	@pd>"20000505" and (((configur? near3 (function or generat$))". ab", ti, "clm.") and (switch near3 matrix))	USPAT	OR	OFF	2002/01/27 11:15
S35	38	(@pd>"20000505" and ((((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) not ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503"))) or (@pd>"20000505" and (((pair or double or two) near5 (block$1 or bank$1)) and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector))))) or (@pd>"20000505" and ((((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)) and ((memory or passgate) near5 (array or vector)))) or (@pd>"20000505" and (((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and ((pair or double or two) near5 (block$1 or bank$1))) and @ad<"19950503")) or (@pd>"20000505" and ((programm$3 near2 (logic or array) or fpga or fga) and ((configur? near3 (function or generat$))".ab", ti, "clm.") and @ad<"19950503")) or (@pd>"20000505" and (((configur? near3 (function or generat$))".ab", ti, "clm.") and (switch near3 matrix)))	USPAT	OR	OFF	2005/09/18 15:01
S38	3	"6417690".pn. or "5850564".pn.	US-PGPUB; USPAT; EPO; DERWENT; IBM_TDB	OR	OFF	2005/09/17 17:17

S40	24	btr.as. and ting.in.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/17 17:19
S41	38207	programm$3 near2 (logic or array) or fpga or fga	US-PGPUB; USPAT; EPO; DERWENT; IBM_TDB	OR	ON	2005/09/17 17:23

PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = TING
First Name = B

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10978269	Not Issued	30	11/01/2004	Computer reader mounting device	TING, BANG-HENG
29167529	Not Issued	164	09/17/2002	CARD READER	TING, BANG-HENG
09519082	Not Issued	160	03/06/2000	High routing architecture in a field programmable gate array	TING, BEN
09745253	Not Issued	160	12/20/2000	Field programmable gate array architecture	TING, BEN
09482149	6462578	150	01/12/2000	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
09955589	6507217	150	09/13/2001	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
09960916	6504399	150	09/24/2001	METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	TING, BENJAMIN S.
10117875	6597196	150	04/05/2002	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
10231320	6624658	150	08/28/2002	METHOD AND APPARATUS FOR	TING, BENJAMIN

				UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	S.
10269364	6703861	150	10/11/2002	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
10412975	6781410	150	04/11/2003	METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	TING, BENJAMIN S.
10428724	6747482	150	05/01/2003	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
10692880	Not Issued	30	10/23/2003	Architecture and interconnect scheme for programmable logic circuits	TING, BENJAMIN S.
10811422	Not Issued	95	03/25/2004	METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	TING, BENJAMIN S.
10814943	Not Issued	95	03/30/2004	SCALABLE NON-BLOCKING SWITCHING NETWORK FOR PROGRAMMABLE LOGIC	TING, BENJAMIN S.
10829527	Not Issued	92	04/21/2004	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
10909810	Not Issued	30	07/29/2004	Interconnection fabric using switching networks in hierarchy	TING, BENJAMIN S.
08101197	5457410	150	08/03/1993	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE	TING, BENJAMIN S.

				LOGIC CIRCUITS	
08186770	Not Issued	166	01/25/1994	APPARATUS AND METHOD FOR PARTITIONING RESOURCES FOR INTERCONNECTIONS	TING, BENJAMIN S.
08229923	Not Issued	166	04/14/1994	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
08433041	Not Issued	166	05/03/1995	SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE	TING, BENJAMIN S.
08434980	5850564	150	05/03/1995	SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE	TING, BENJAMIN S.
08484922	Not Issued	164	06/07/1995	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
08506828	5640344	150	07/25/1995	PROGRAMMABLE NON-VOLATILE BIDIRECTIONAL SWITCH FOR PROGRAMMABLE LOGIC	TING, BENJAMIN S.
08534500	Not Issued	161	09/27/1995	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
08599122	5640327	150	02/09/1996	APPARATUS AND METHOD FOR PARTITIONING RESOURCES FOR INTERCONNECTIONS	TING, BENJAMIN S.
08708403	6034547	150	09/04/1996	METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	TING, BENJAMIN S.

08909928	6051991	150	08/12/1997	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
08951814	6088526	150	10/14/1997	SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE	TING, BENJAMIN S.
09028769	Not Issued	161	02/24/1998	ARCHITECUTRE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
09034769	6433580	150	03/02/1998	ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
09089298	6417690	150	06/01/1998	FLOOR PLAN FOR SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE	TING, BENJAMIN S.
09243998	6329839	150	02/04/1999	METHOD AND APPARATUS FOR UNIVERSAL PROGRAM CONTROLLED BUS ARCHITECTURE	TING, BENJAMIN S.
09255026	Not Issued	161	02/22/1999	SEMI-HIERARCHICAL REPROGRAMMABLE FPGA ARCHITECTURE	TING, BENJAMIN S.
09377304	6300793	150	08/18/1999	SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE	TING, BENJAMIN S.
09467736	6320412	150	12/20/1999	ARCHITECTURE AND INTERCONNECT FOR PROGRAMMABLE LOGIC CIRCUITS	TING, BENJAMIN S.
07752282	Not Issued	166	08/29/1991	CONFIGURABLE LOGIC ARRAY	TING, BENJAMIN SHIU-MING
08014179	Not Issued	161	02/05/1993	REPEATERS WITH EXPRESS/LOCAL BUS PAIRS IN A	TING, BENJAMIN SHIU-MING

				CONFIGURABLE LOGIC ARRAY	
10021744	Not Issued	30	12/05/2001	Floor plan for scalable multiple level tab oriented interconnect architecture	TING, BENJAMINS S.
09828547	6925646	150	04/06/2001	INHERITANCE OF OBJECT'S PROPERTIES AND OUT OF DIFFERENT APPLICATION CONTEXTS IN PROPERTIES FILE OBJECTS	TING, BENNETT
60198718	Not Issued	159	04/20/2000	Inheritance of object's properties in and out of different application contexts in properties file objects	TING, BENNETT
60205700	Not Issued	159	05/19/2000	Inheritance of object's properties in and out of different application contexts in properties file objects	TING, BENNETT
09191471	Not Issued	161	11/12/1998	DISTRIBUTED, HIGH PERFORMANCE ARCHITECTURE FOR ONLINE INVESTMENT SERVICES	TING, BENNETT L. W.
09759573	Not Issued	160	01/12/2001	Content serving method and system	TING, BENNETT LI WEN
09759922	Not Issued	160	01/12/2001	Content serving method and system	TING, BENNETT LI WEN
29111473	D425045	150	09/29/1999	INTERFACE CARD	TING, BENNY
29135144	Not Issued	164	01/05/2001	Telephone handset	TING, BENNY
29135145	Not Issued	164	01/05/2001	Base	TING, BENNY
09746646	Not Issued	161	12/21/2000	Sports shoe	TING, BERNARD
10684833	Not Issued	71	10/14/2003	Mixing device	TING, BIE DAO

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#1	(((ting<in>metadata) <and> (fpga<in>metadata))) <and> (pyr >= 1951 <and> pyr <= 1995)
#2	(((layers <in>metadata) <and> (fpga<in>metadata))<and> (dimnsiona<in>metadata)) <and> (pyr >= 1951 <and> pyr <= 1995)
#3	(((layers <in>metadata) <and> (fpga<in>metadata))<and> (dimensiona<in>metadata)) <and> (pyr >= 1951 <and> pyr <= 1995)
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#11	(((layers<in>metadata) <and> (fpga<in>metadata))<and> (dimensions<in>metadata)) <and> (pyr >= 1951 <and> pyr <= 1995)